

FIG.1A

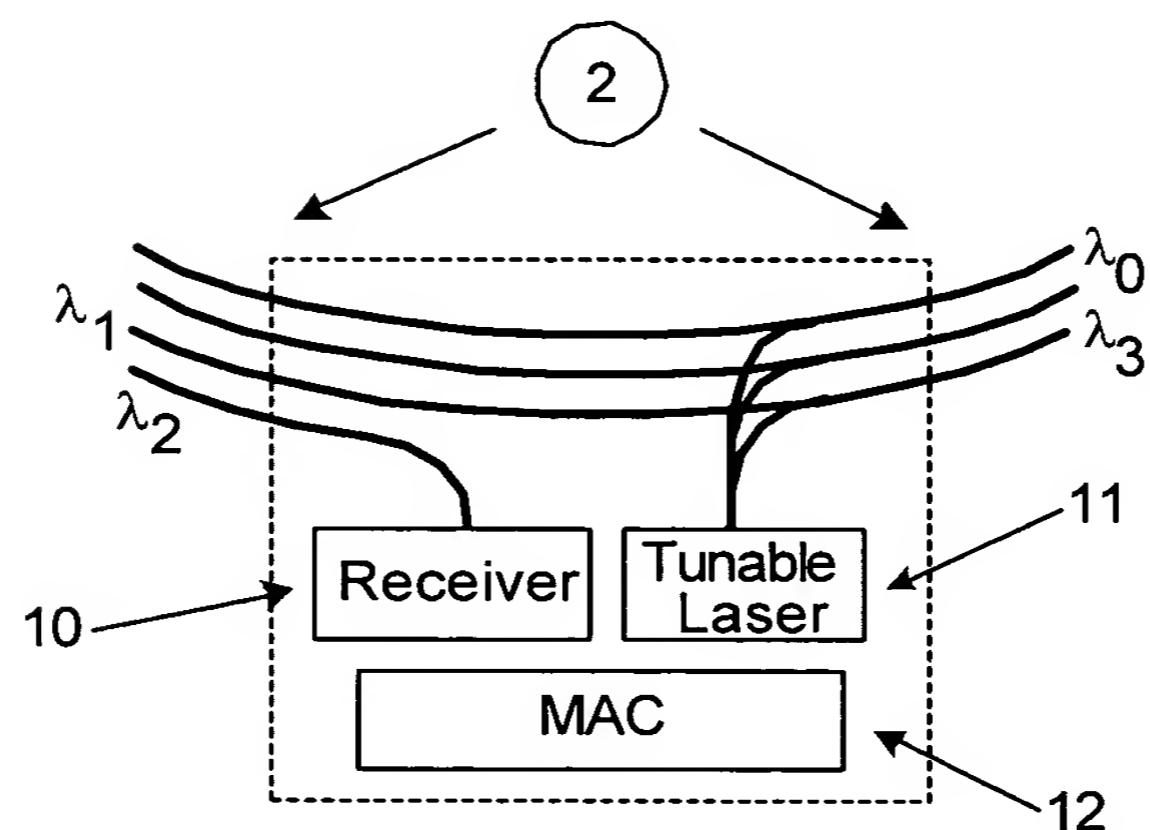


FIG.1B

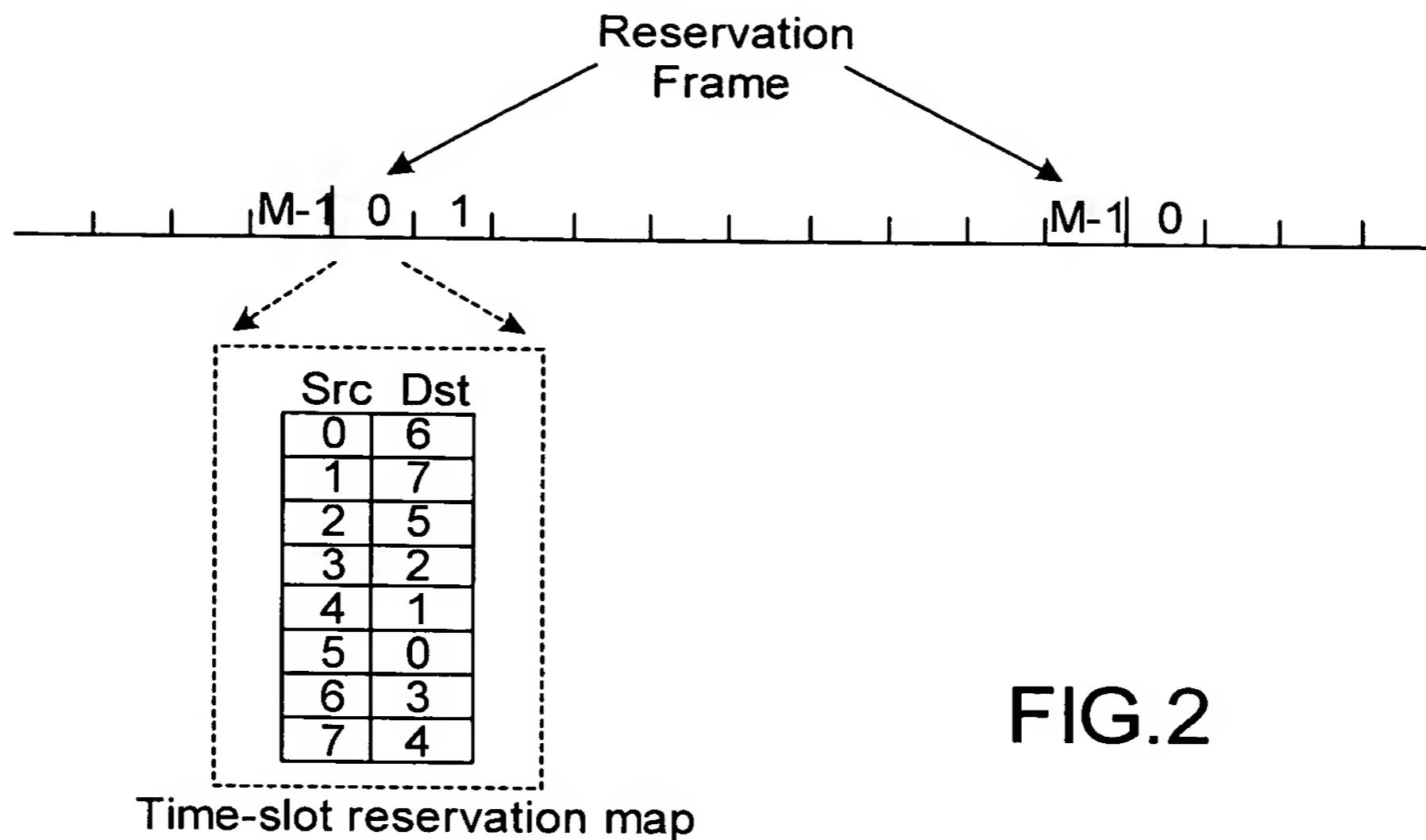
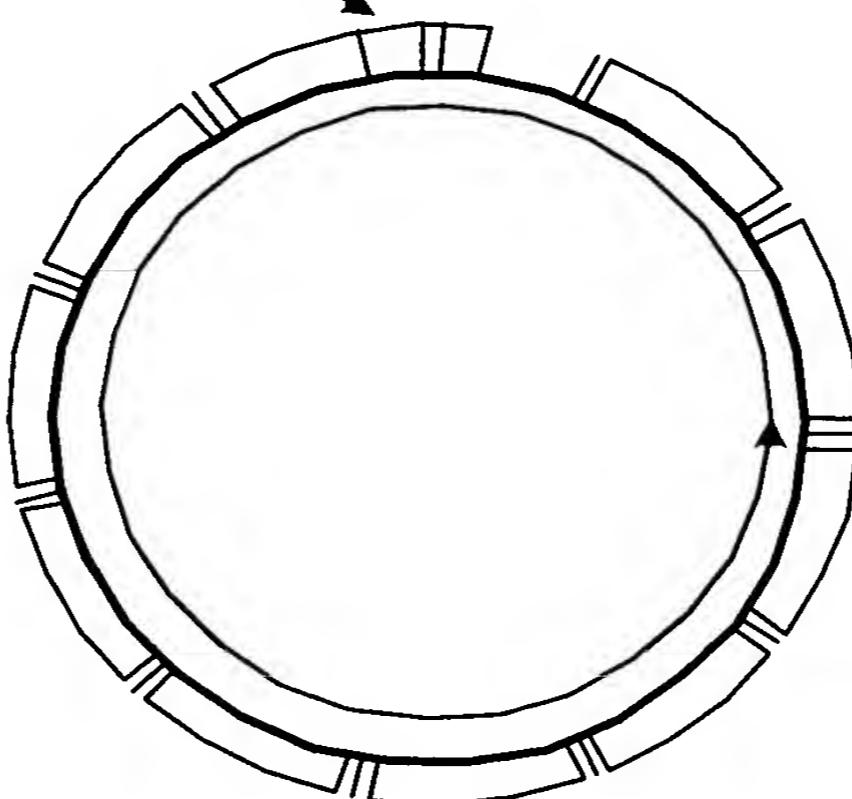


FIG.3

Time-slots overlap



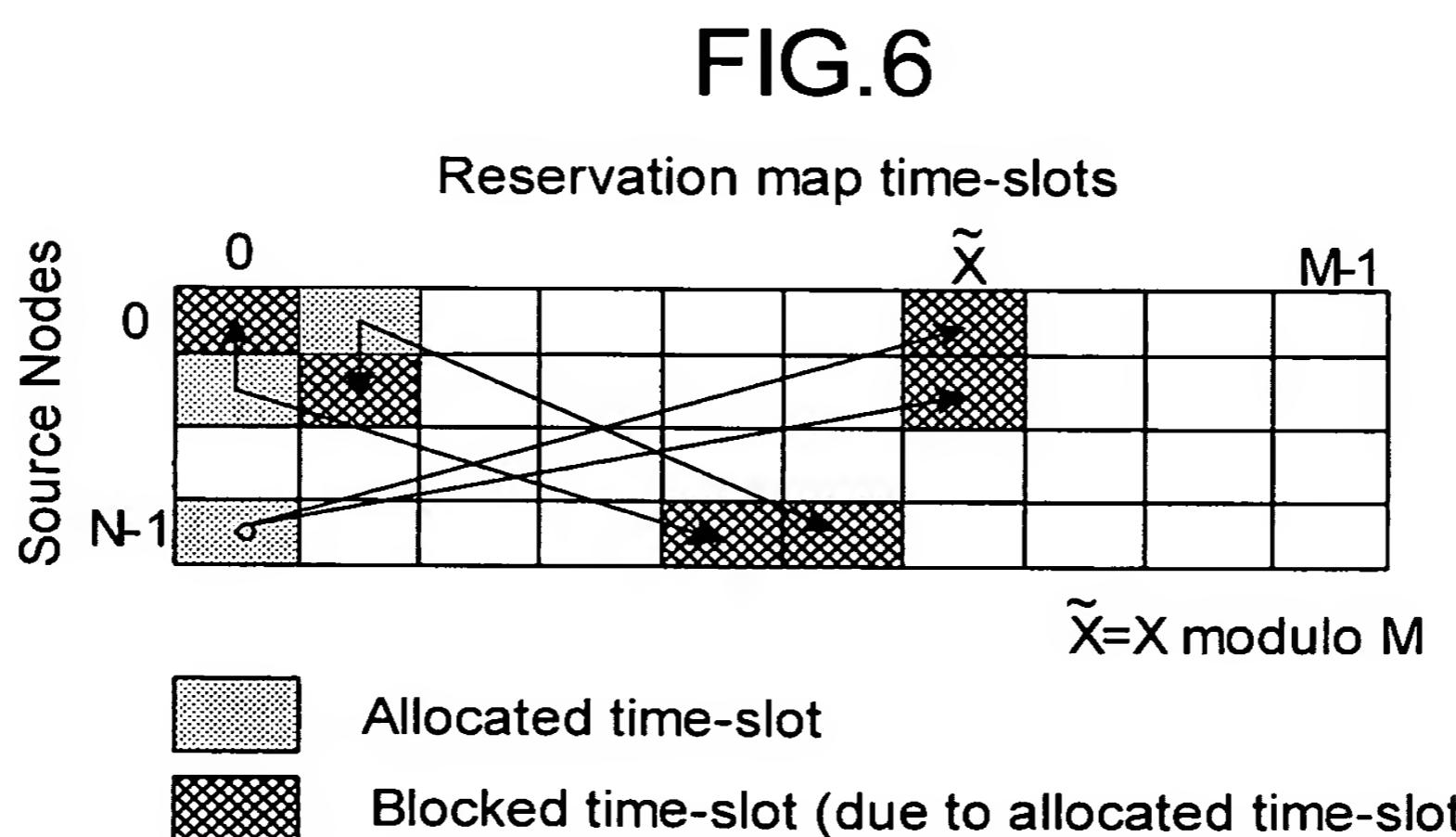
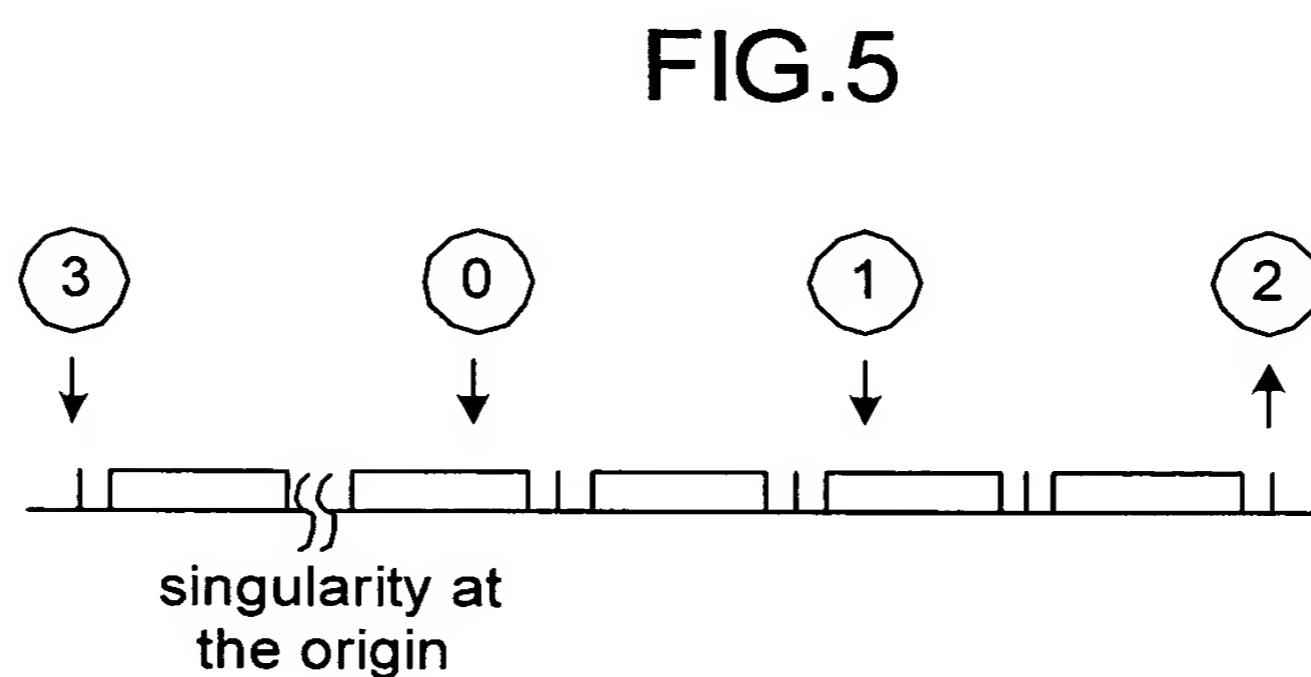
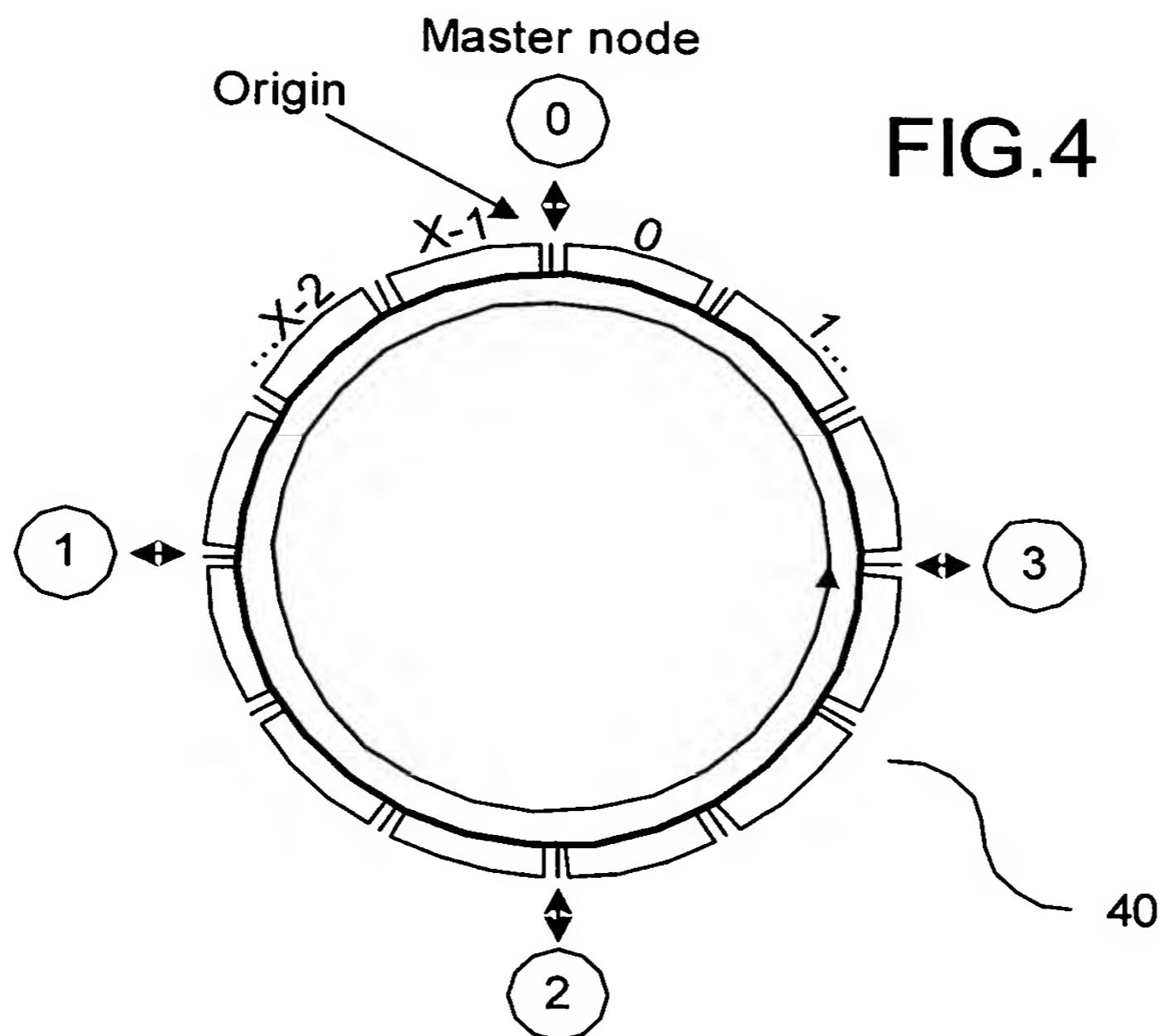


FIG. 7

Destination Nodes				
Source Nodes	0			
	0	0		
		0		
			0	
				0

FIG.8

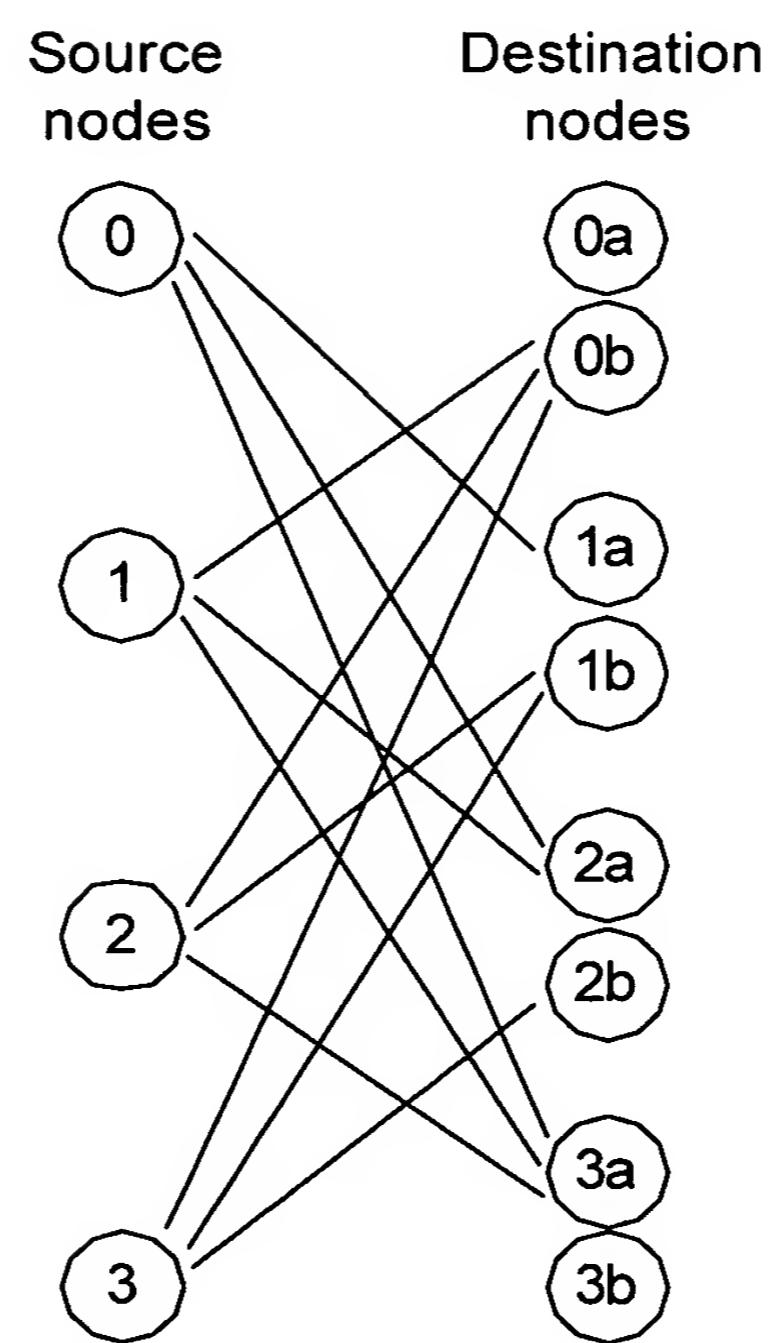


FIG.9

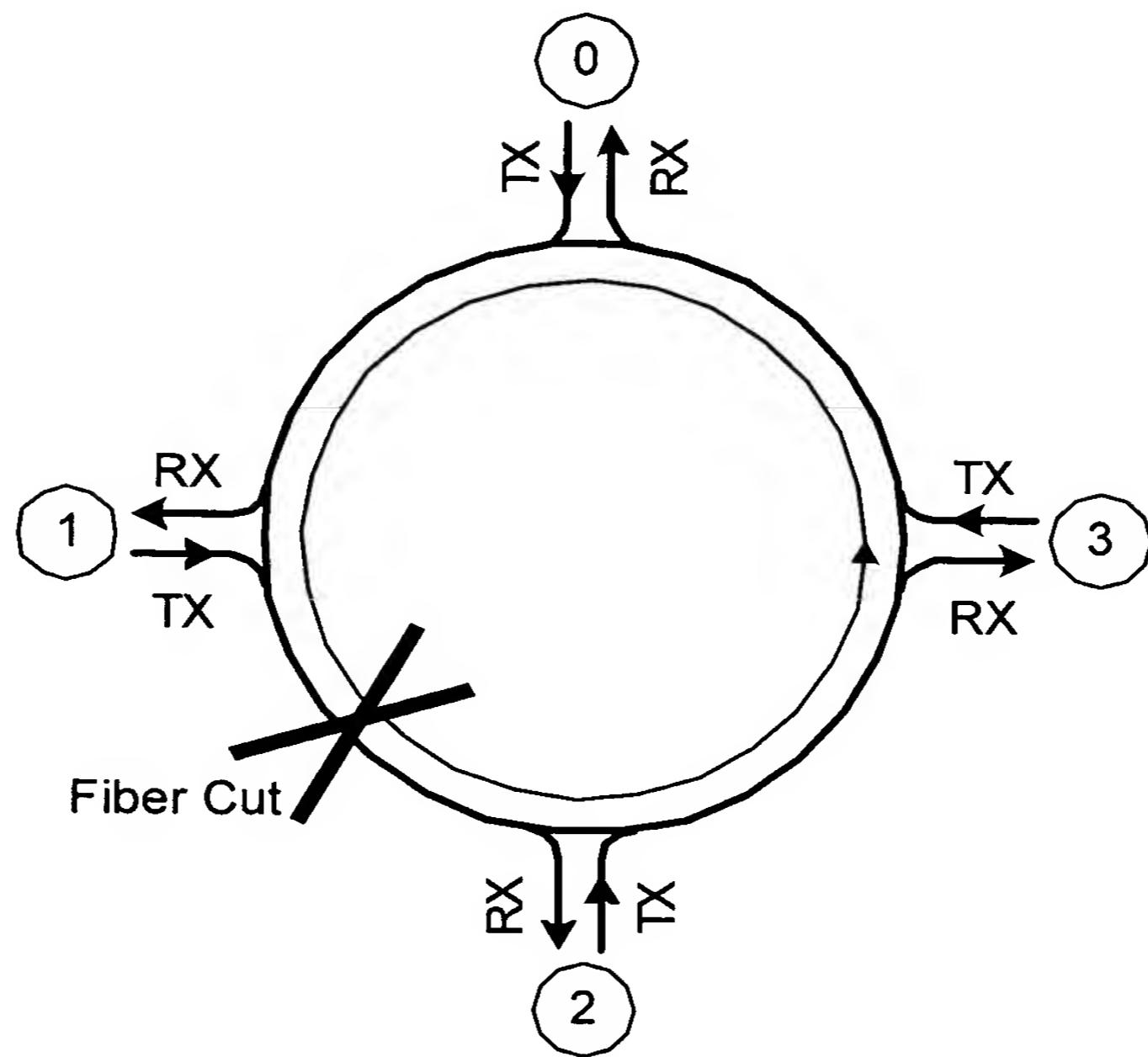


FIG.10

Node Transmitting
slot clock

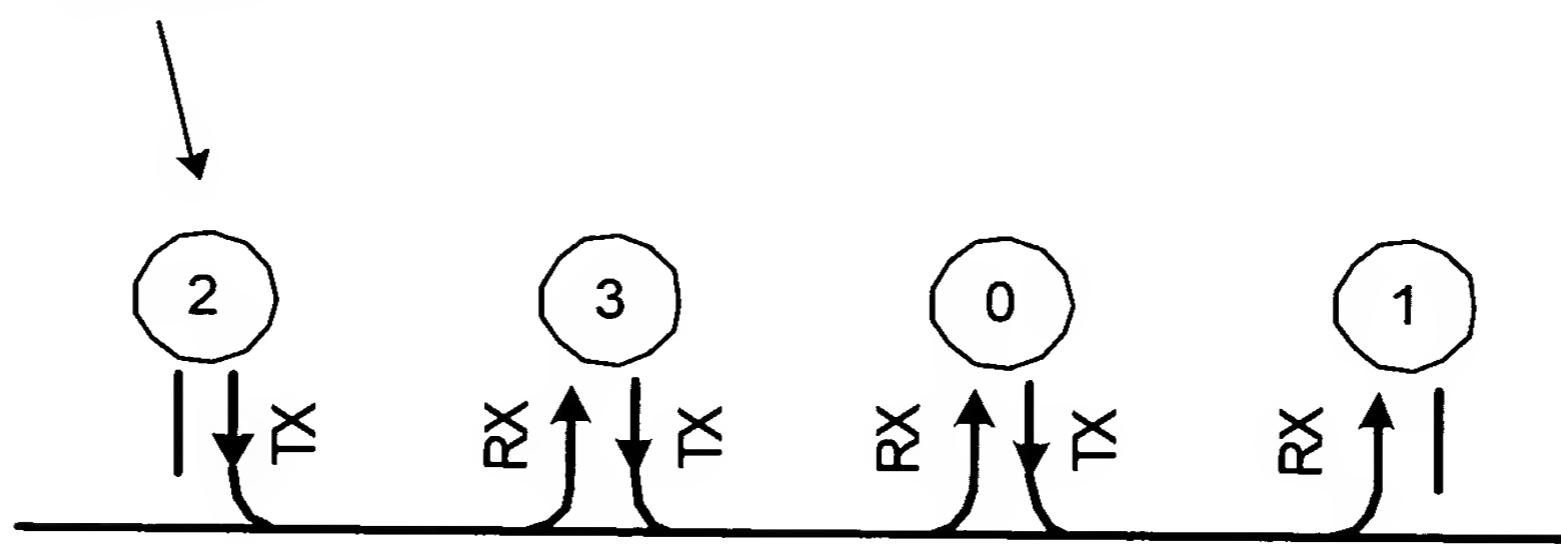


FIG.11

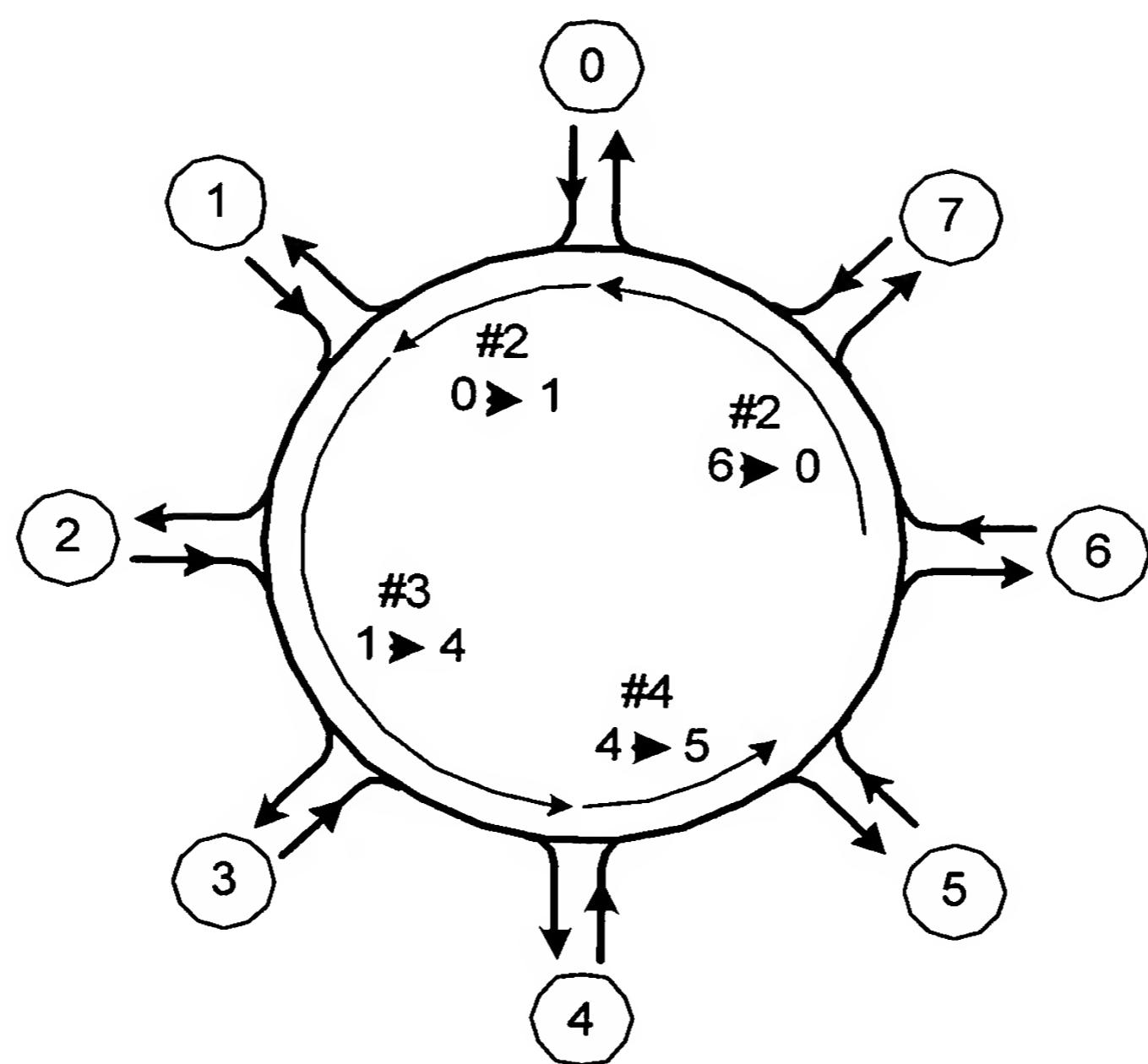


FIG.12

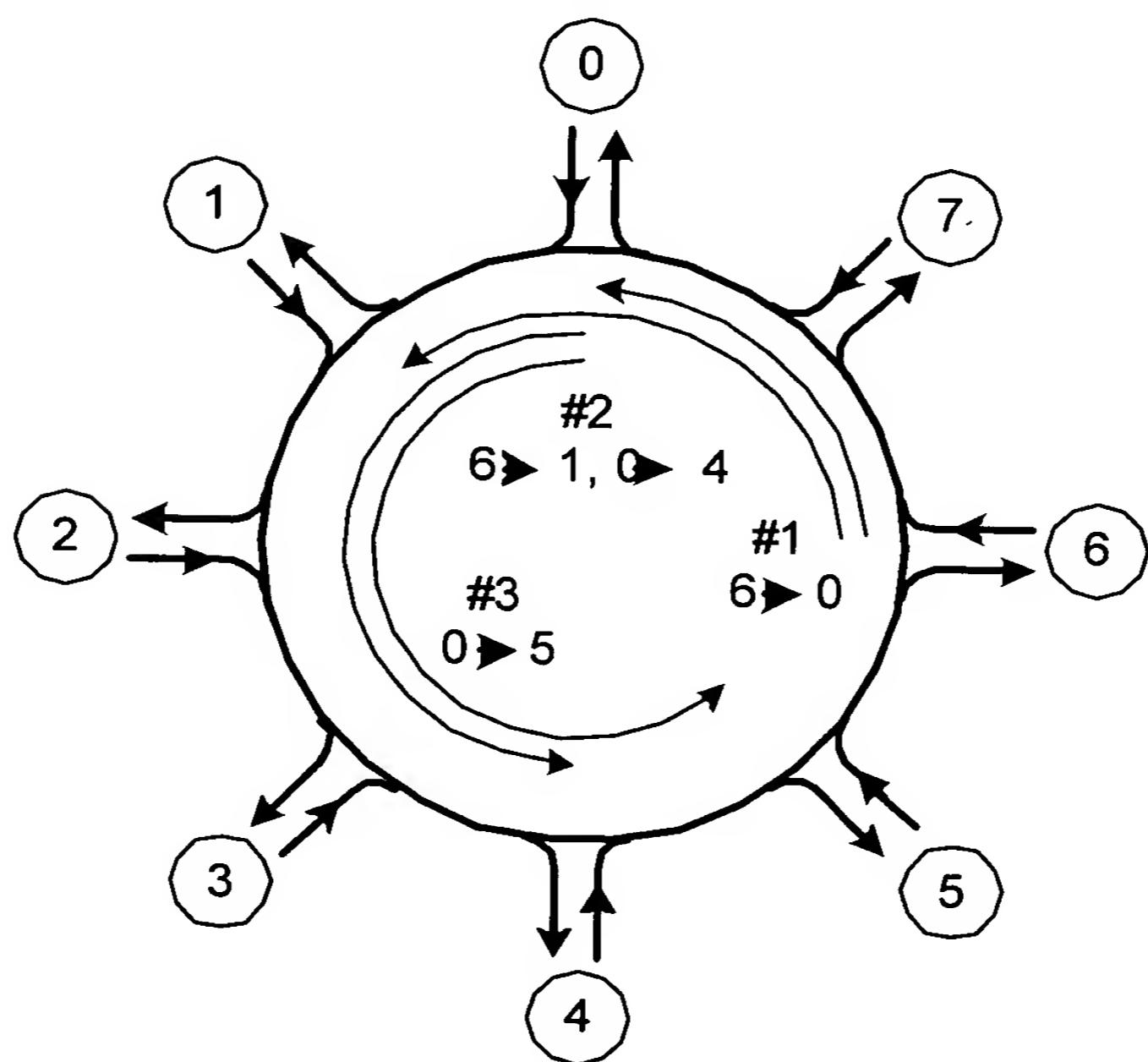


FIG.13

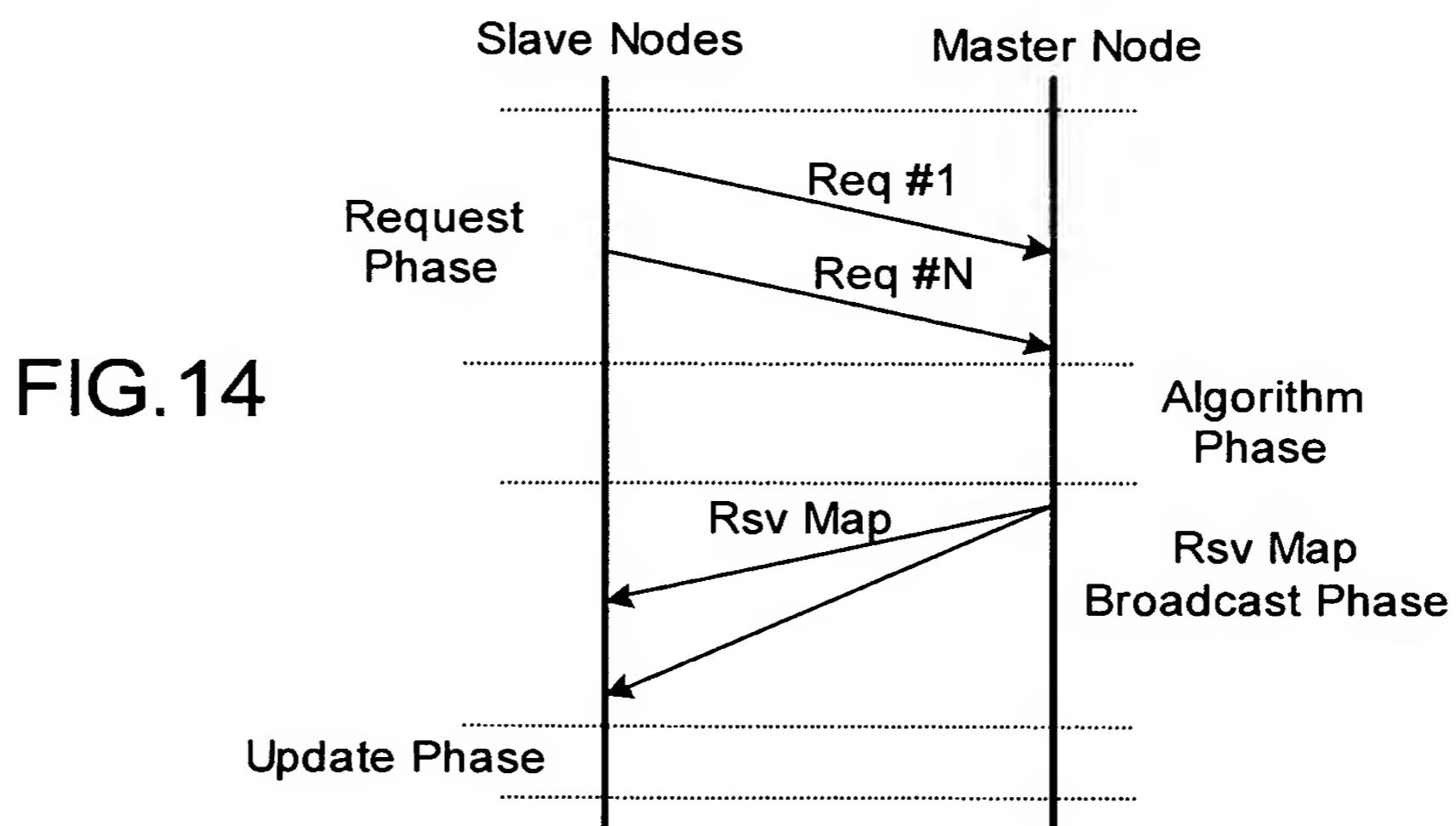
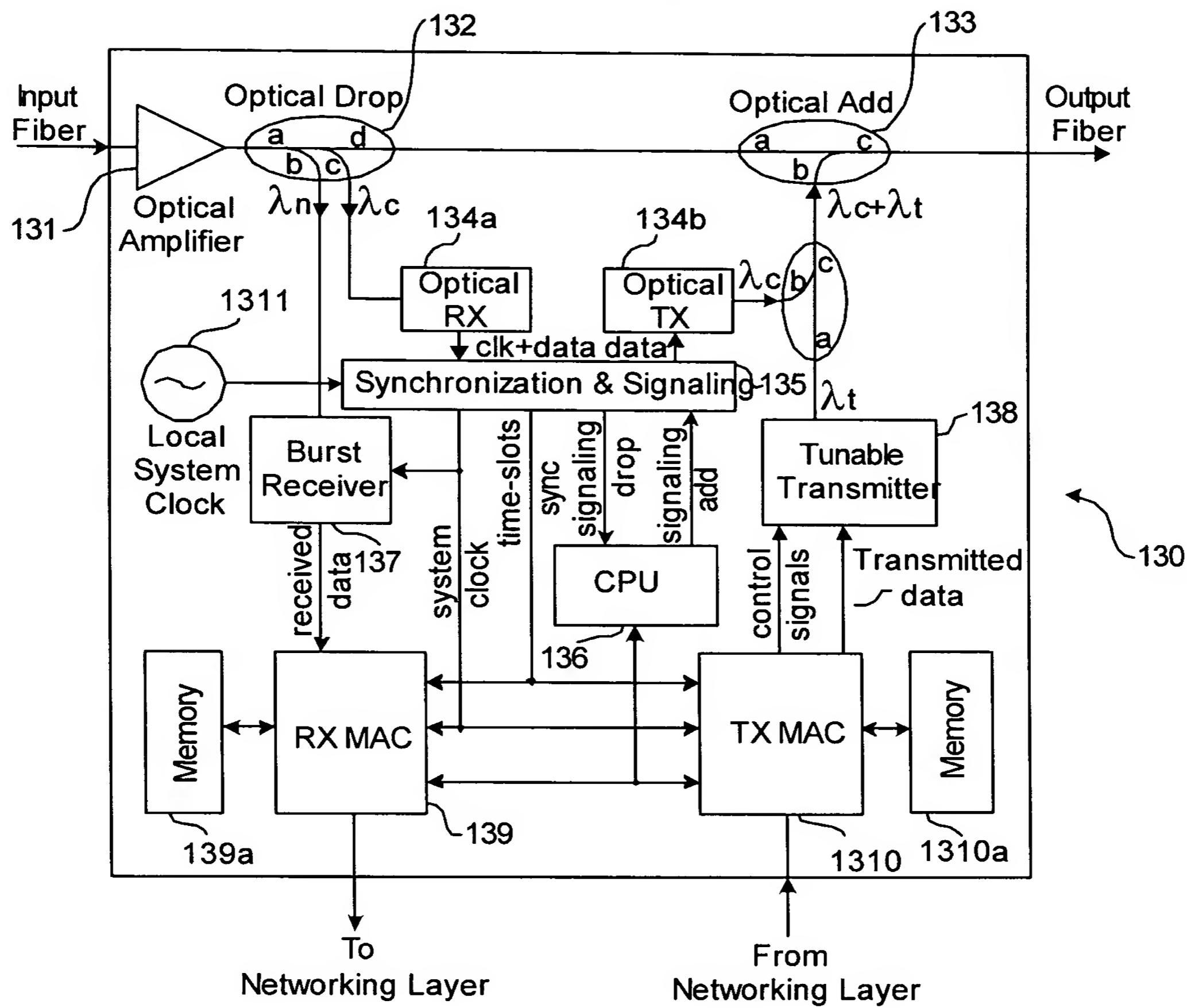


FIG.14

FIG.15

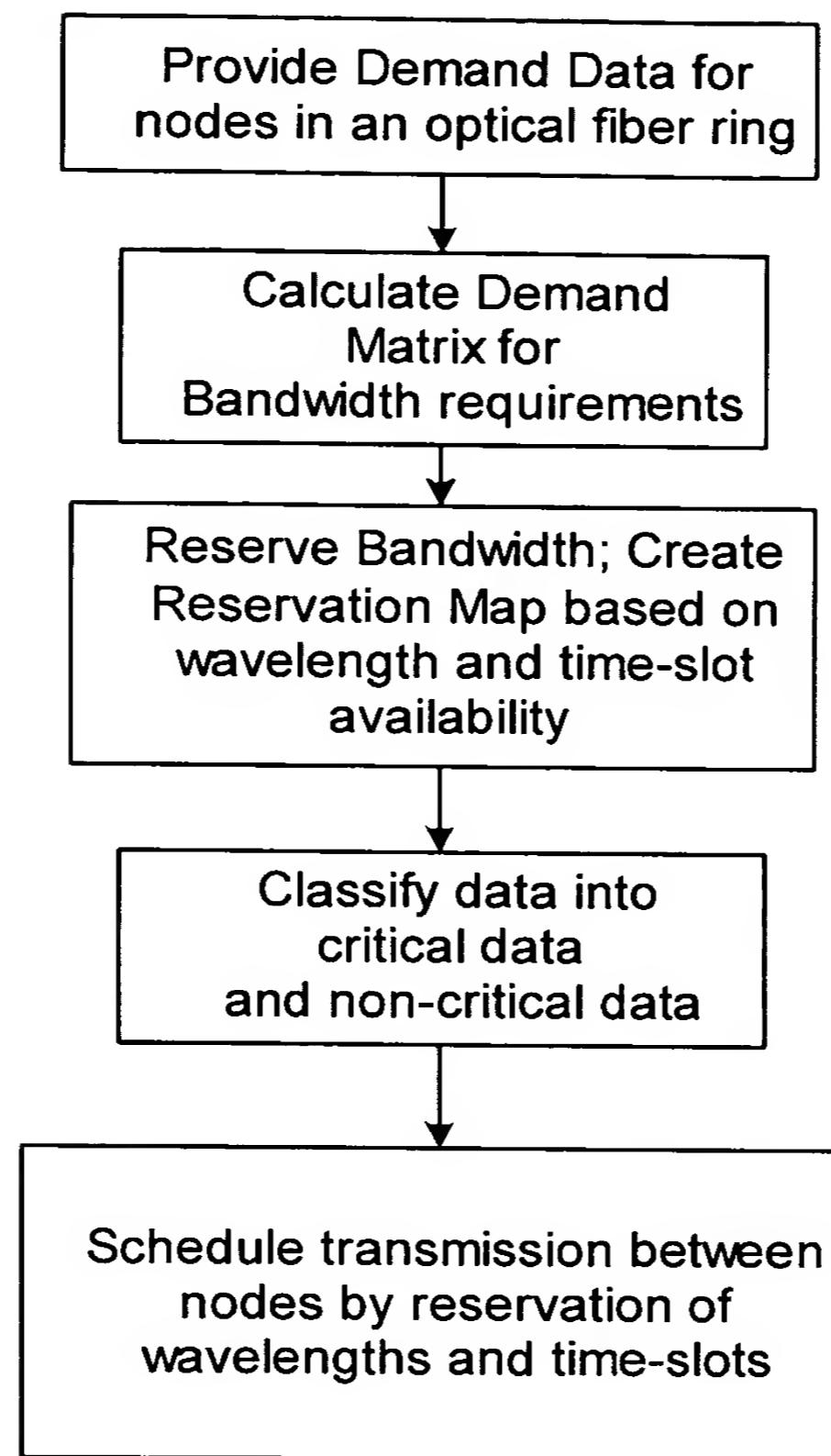
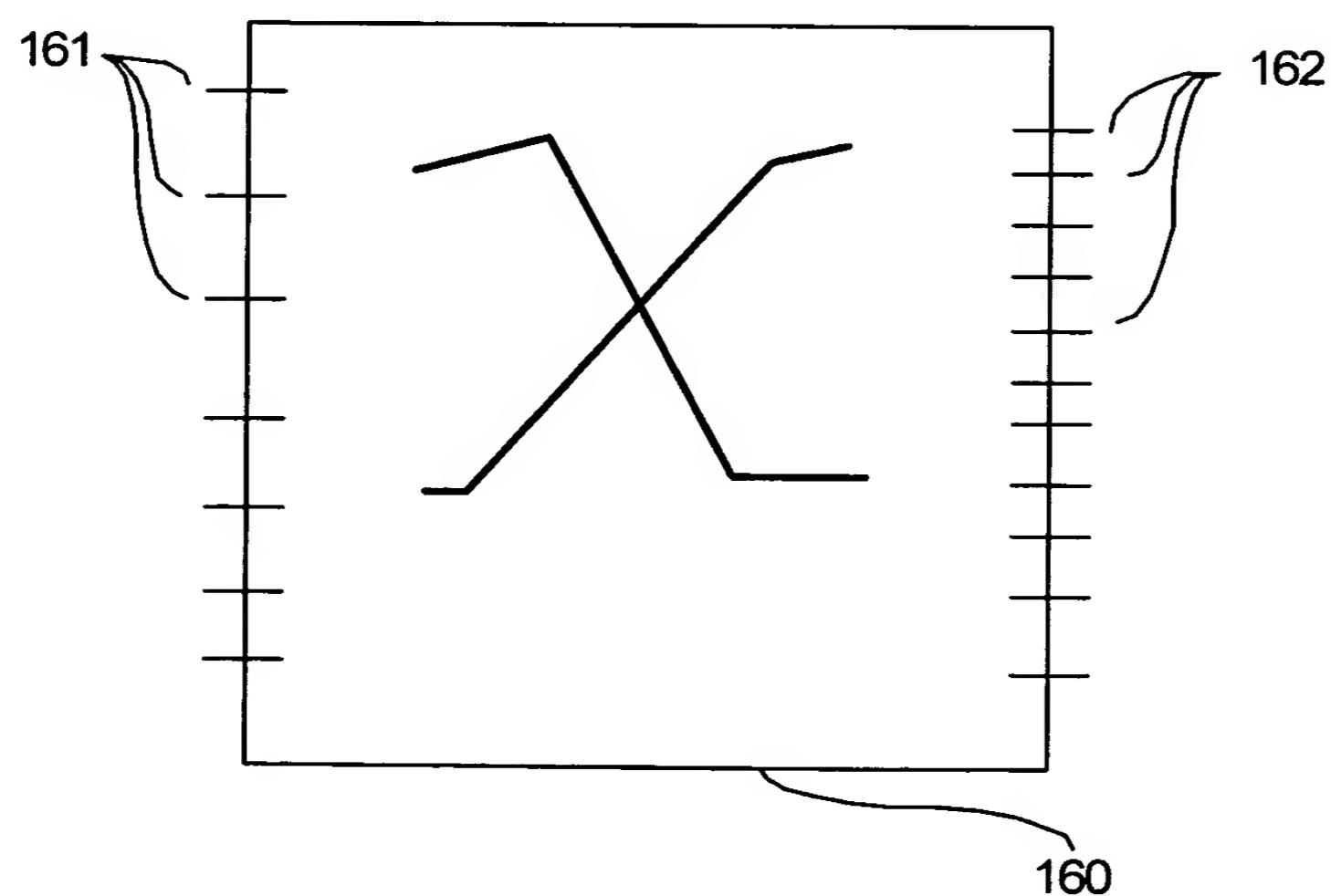


FIG.16



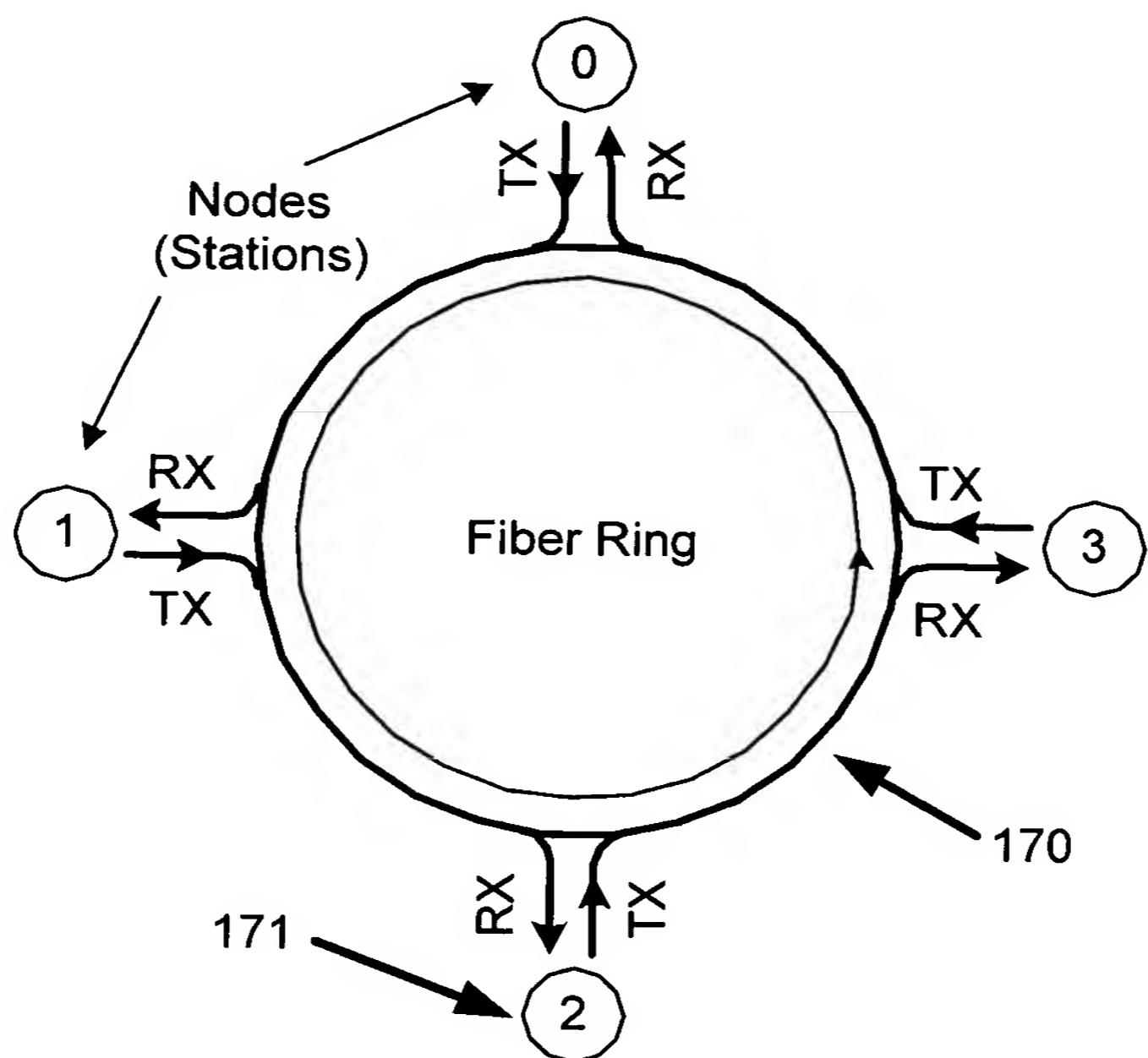


FIG.17A

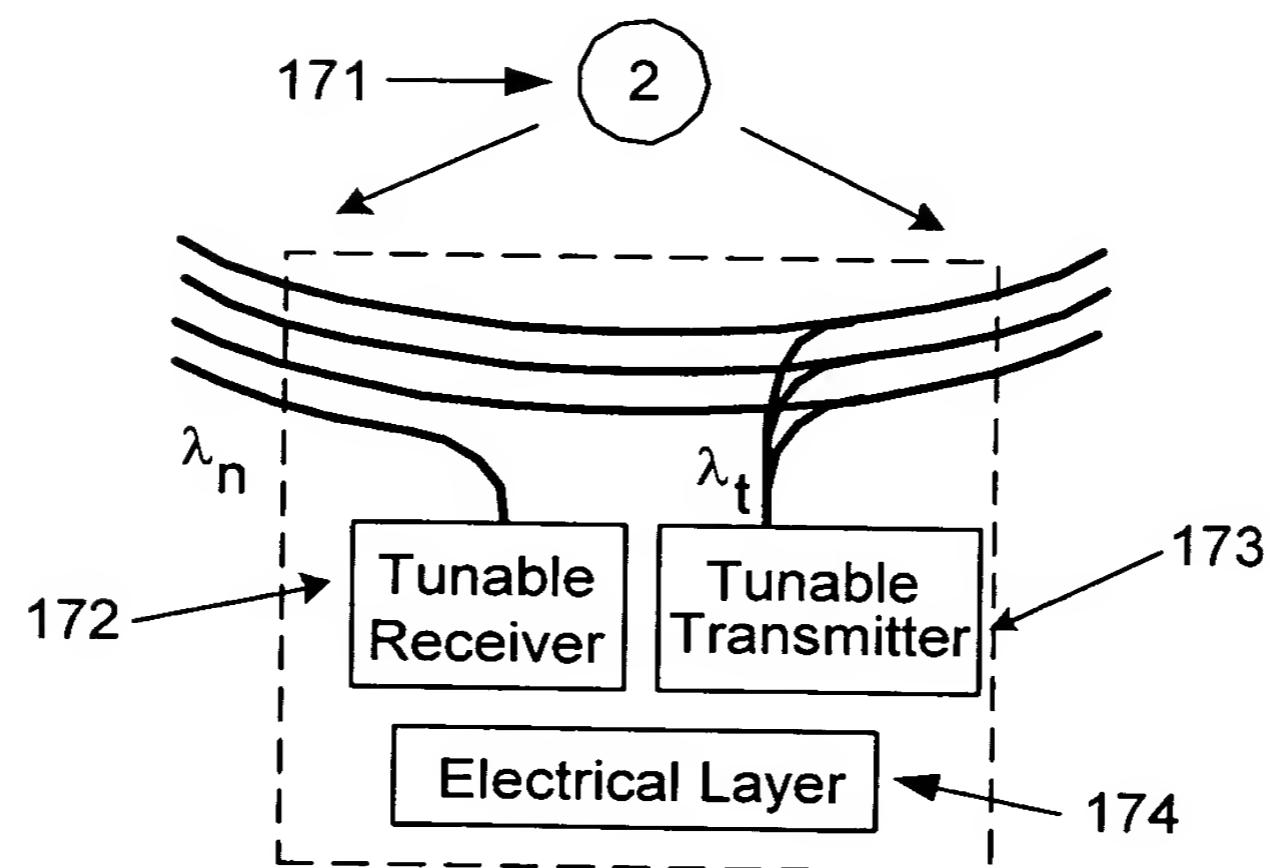


FIG.17B

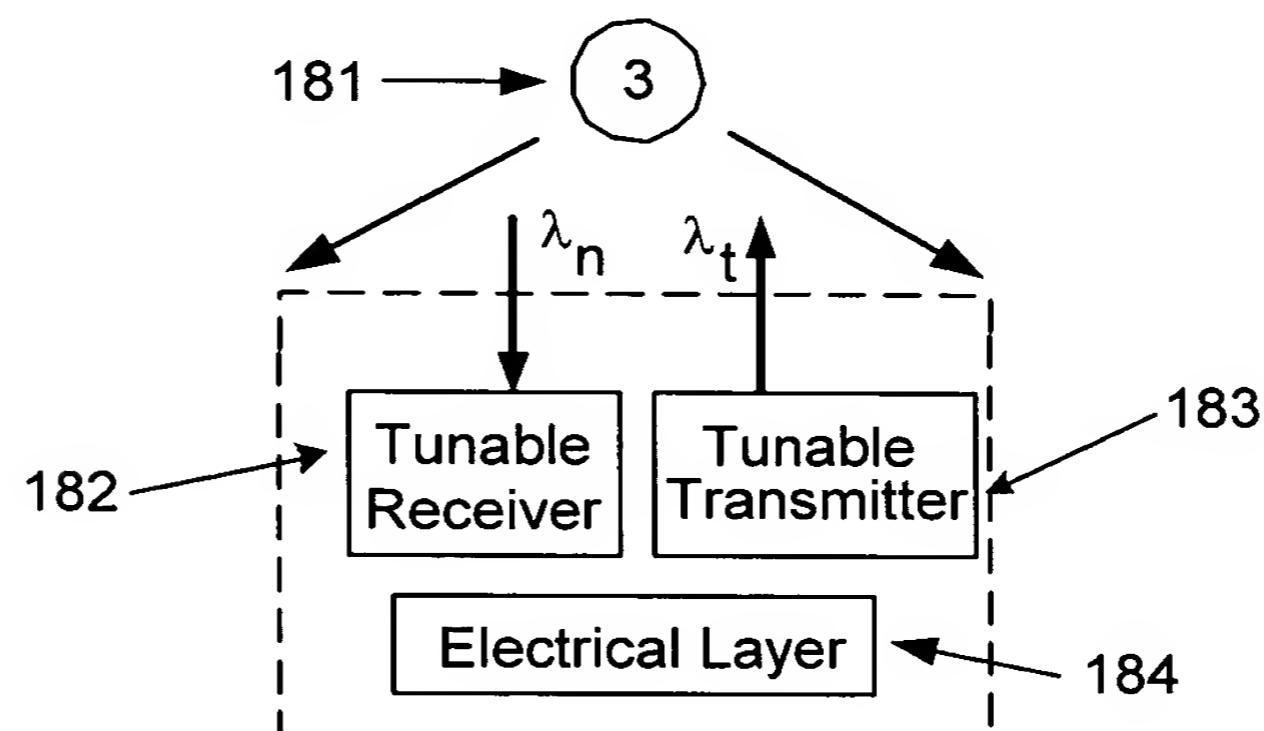
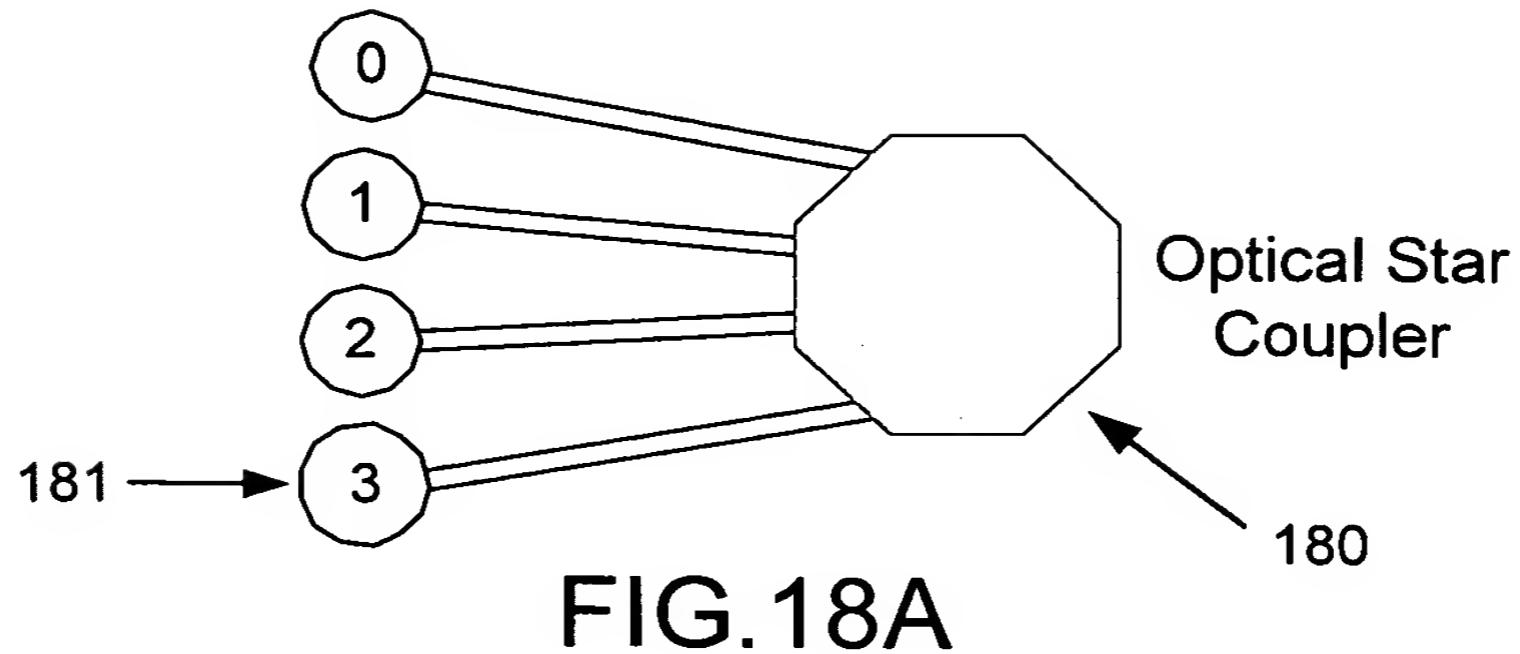


FIG.18B

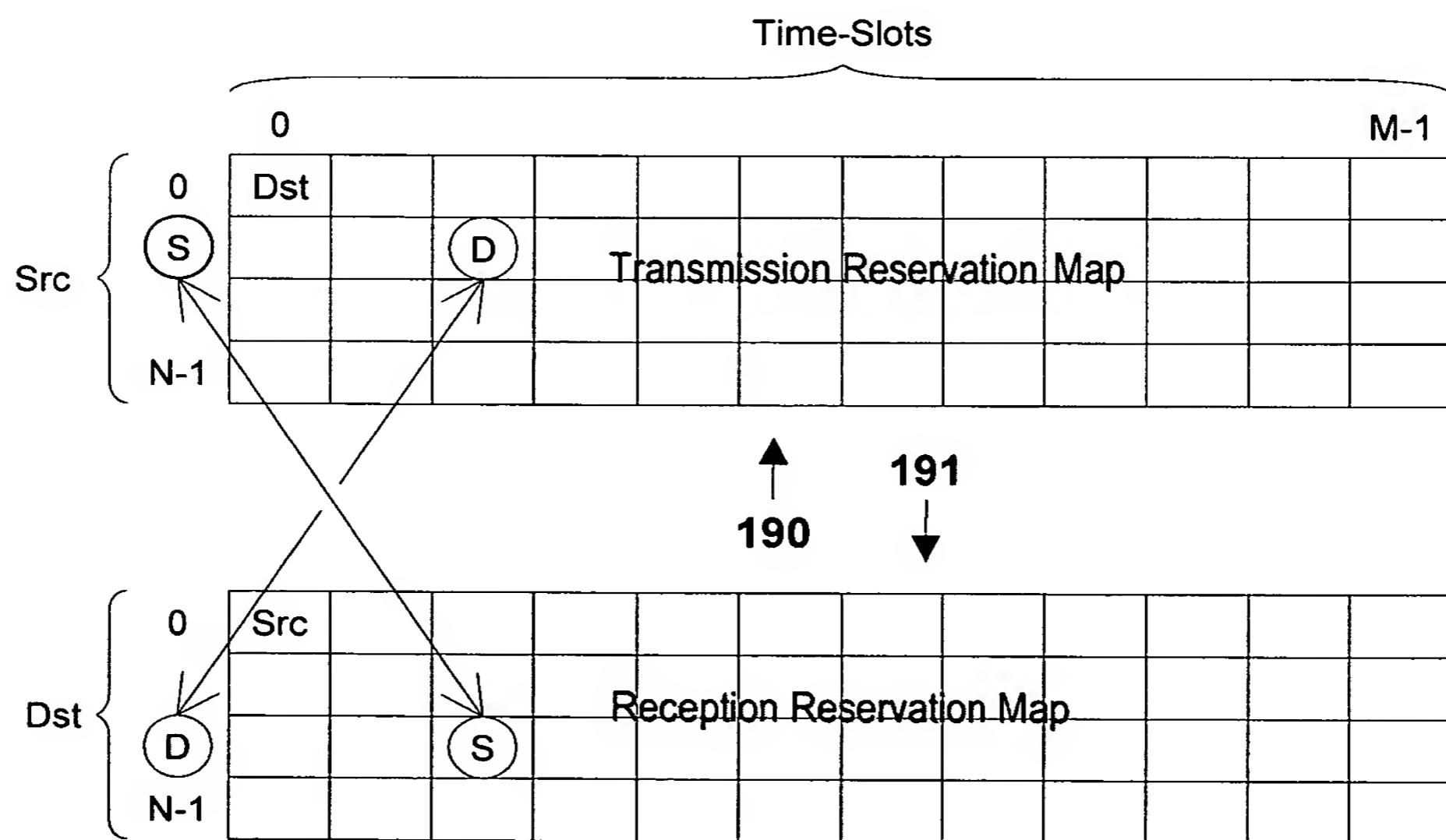


FIG.19

